A NEW APPROACH TO ACTIVE PHASED ARRAYS THROUGH RF-WAFER SCALE INTEGRATION*

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ABSTRACT

This paper describes a new approach to active phased array technology. Here, several modules are fabricated at the same time and placed in a layered structure. The layers include the RF modules, cooling manifold, dc bias distribution, RF manifold, and radiating elements. In this configuration, 16 or more T/R modules are fabricated on a single 3-inch GaAs wafer. The realization of multiple modules on a wafer is made possible by redundancy of circuit elements and novel mechanical switches. Preliminary results on these efforts are presented.

INTRODUCTION

For the past 3 years the Westinghouse Electric Corporation, with support from the McDonnell Douglas Corporation, has been pursuing a new technology which promises to expand the applicability of active phased antennas and to drastically reduce their cost. The concept is called RF-Wafer Scale Integration. In this technology, several T/R modules are fabricated on a 3-inch GaAs wafer. A configuration containing 16 such cells is shown in figure 1. As shown, each T/R module is chosen to be no larger than a half wavelength, $\lambda/2$, at the highest operating frequency. The configuration of active T/R modules is mounted to the substrate assembly and becomes a layer within an overall package which forms an active radiating subarray as shown in figure 2. In April 1989, the Defense Advanced Research Projects Agency (DARPA) awarded a 2-year program to Westinghouse to demonstrate the RF-wafer scale concept in the 2- to 12-GHz range with goals of extending performance to 2 to 20 GHz. In the present feasibility demonstration program, effort is being directed to achieving a transmitter power at about the 1/2- to 1-watt level at broadband frequency segments within the overall 2- to 12-GHz range. While not satisfying all active phased array needs, the program is addressing a range of possible applications. Some of these are listed in figure 3. In the following sections of this paper, efforts to date in the device/circuit area and in the antenna integration areas are described.

SYSTEMS APPLICATION

The advantages of active phased antennas are well known for military radar, EW, and communications/navigations systems. To date, the one major deterrent to such systems has

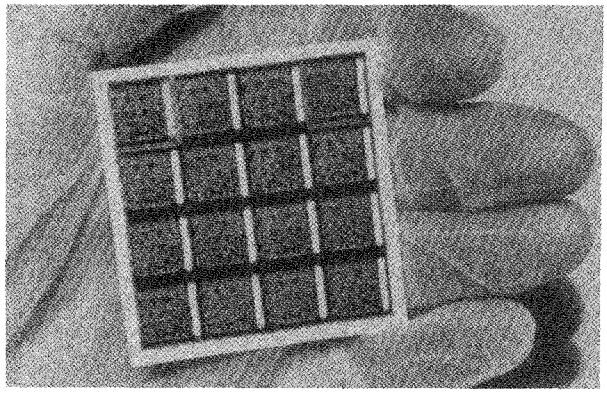

Figure 1. Three-Inch GaAs Wafer That Contains 16 T/R Cells

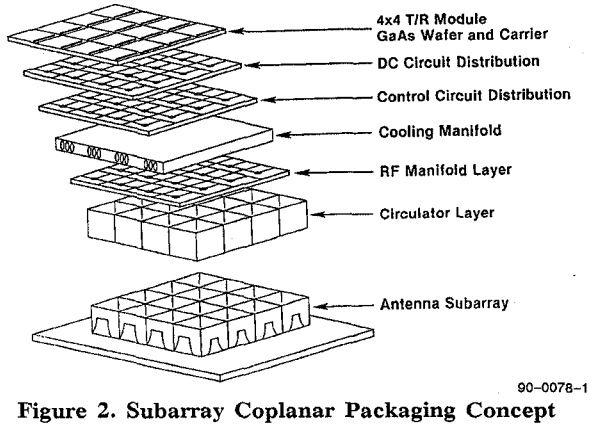

Figure 2. Subarray Coplanar Packaging Concept

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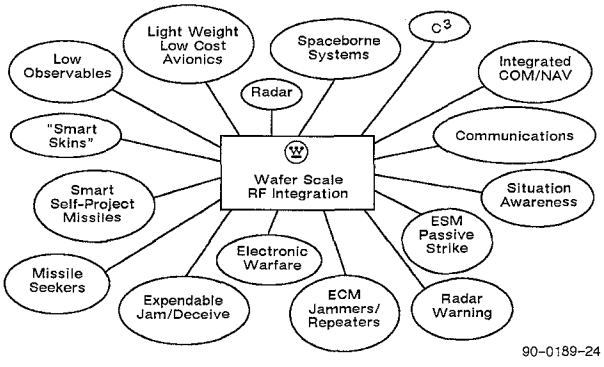

Figure 3. Potential Applications of RF-Wafer Scale Integration Technology

been the cost of fabricating and arraying large numbers of individual T/R modules into a large antenna face (up to 2000 to 4000 modules for radar applications). Additionally, for airborne applications, present structural shapes dictate that the antenna structure be conformal to the airframe surface. The RF-wafer scale concept provides an approach to solving both of these problems. First, individual T/R modules are eliminated and are replaced by a multielement subarray. Second, a thin subarray structure results which may be flush-mounted or incorporated into a vehicle's surface.

A large percentage of present and future systems applications are in the 2- to 20-GHz region of the spectrum. This range has been chosen for the RF-wafer scale feasibility demonstration program.

As described later, the radiated power output for a single cell and the noise figure of its receive channel have been selected to be compatible with the fabrication technique of ion implantation into GaAs wafers. The targeted parameters are compatible with many of the system needs within the targeted frequency range.

SUBARRAY ARCHITECTURE

A basic T/R module circuit diagram is shown schematically in figure 4. Here the transmit amplifier usually requires three to four stages of amplification to obtain the required gain of 25 to 30 dB. A similar number of gain stages are required in the LNA chain. Figure 5 shows a state-of-the-art module which contains nine GaAs chips along with associated control circuits. In this structure an input signal enters on the right and emerges on the left. In the RF-wafer scale architecture, individual T/R module circuits are included in a single $\lambda/2 \times \lambda/2$ cross section. Adjacent $\lambda/2 \times \lambda/2$ T/R cells surround the individual T/R cell until a subarray consistent with the GaAs wafer size is realized. A 4 x 4 T/R cell or 16-element subarray is presently being addressed. The subarray is cut from the wafer to form the basic GaAs subarray layer. Additional layers are sandwiched above the GaAs layer as were shown in figure 2. These layers include:

- GaAs layer
- Cooling layer or manifold
- dc bias circuits
- RF feed structure
- Control circuits
- Antenna radiating elements.

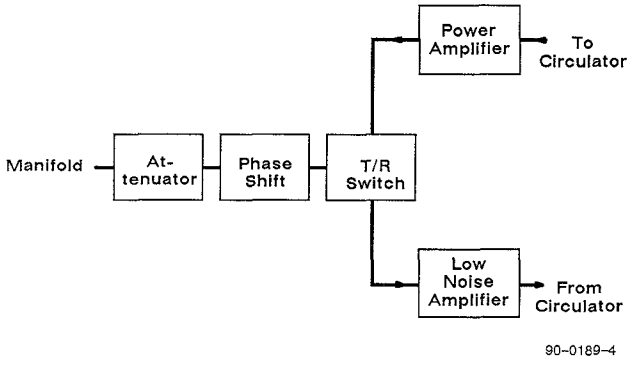

Figure 4. Block Diagram of RF-Wafer Scale T/R Cell

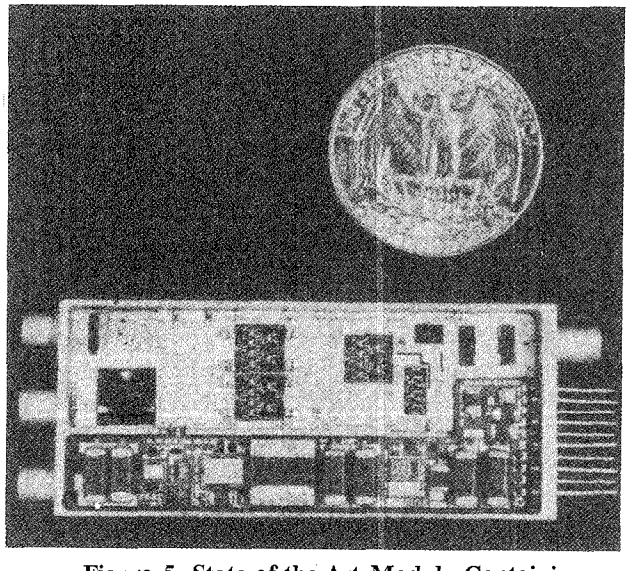

Figure 5. State-of-the-Art Module Containing Nine GaAs Chips

This implementation requires thermal, dc, and RF feedthroughs through the various layers. The layers must be thermally matched to prevent deformation or cracking as thermal cycling occurs. Figure 6 is a cross-sectional drawing of the actual implementation of the structure used while figure 7 shows the GaAs wafer segment bonded to the layered assembly.

REALIZATION OF GaAs T/R CELLS

The realization of large area GaAs chips with high yield has for some time represented a technical challenge. In fact, only limited success has been achieved for a single module on the chip. The prospect of realizing several adjacent functional T/R modules has been made possible by two important breakthroughs. These include:

- Realization of nearly damage-free GaAs wafer surface[1]
- Development of mechanical switches which allow for redundancy in device/circuit elements within the T/R cell.

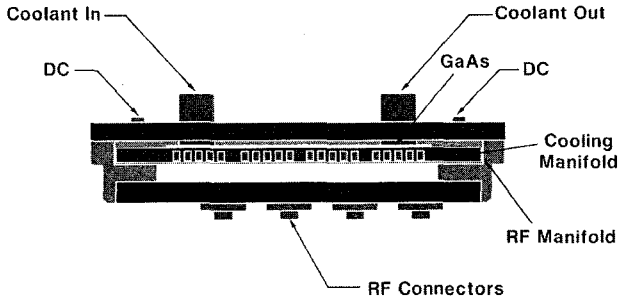

Figure 6. T/R Subassembly - Side View

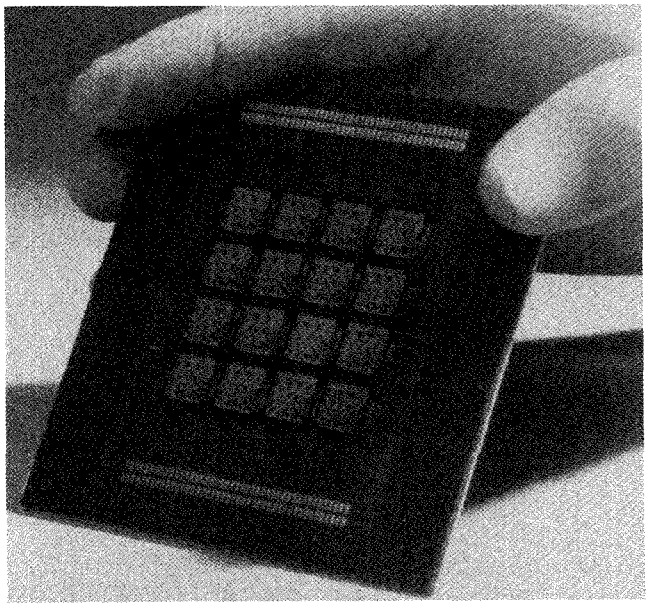

Figure 7. GaAs Wafer Mounted to Layered Structure

A T/R module cell that was developed on the company-supported program is shown in figure 8, while a closeup of the mechanical switch is shown in figure 9. The mechanical switches are formed by fabricating airbridges that are open at one end and cantilevered over the adjacent transmission line. They are closed by using a suitable wedge bonding tool. As shown for transmit, each stage of amplification is repeated three times. After wafer level probing, the "best" performing stages are selected and suitable switches are permanently closed to complete the desired amplifier chain. For receive, two of six LNA gain stages are selected. Other circuit elements are listed on the figure.

The development of improved wafer polishing techniques has resulted in nearly damage-free wafers. These are the key to the high yields for RF-WSI. Damage-free wafers have resulted in nearly a doubling of yield for small-to-medium-sized devices.

The present wafer scale program uses the following:

- Selective ion implantation into 3-inch LEC damage-free wafers
- 0.5μ e-beam written gates with stepper lithography
- Double and triple circuit/device redundancy.

The electrical specification goals for an individual T/R cell are:

Transmit:	Bandwidth	6 to 12 GHz
	Radiated Power	0.5 watt
	Phase Bits	6
	Amplitude Bits	5
Receive:	Bandwidth	4 to 12 GHz
	Noise Figure	< 7 dB
	Gain	> 20 dB

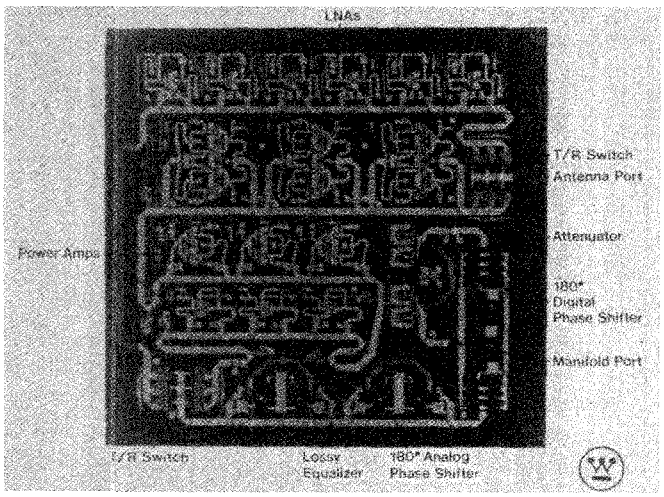

Figure 8. RF-WSI T/R Cell Layout

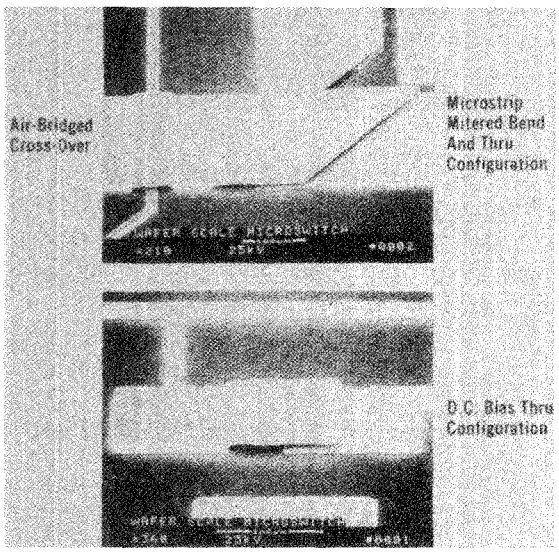

Figure 9. RF-WSI Mechanical Switches

ANTENNA INTEGRATION

In addition to realization of the GaAs T/R cells, the complex packaging containing the RF manifold, dc bias circuits, controller, necessary cooling, and the radiating elements must be assembled into a single structure. Both dc and RF signal corrections must be made through the various layers. Figure 10 shows a large via hole which has been formed from multiple laser drilling and wet etching through a 0.010-inch GaAs substrate. Metallization is then applied. Such vias have exhibited over 97% yields across a 3-inch wafer. Theoretical and experimental studies are presently underway to determine optimum configurations for the radiating element and the additional layers.

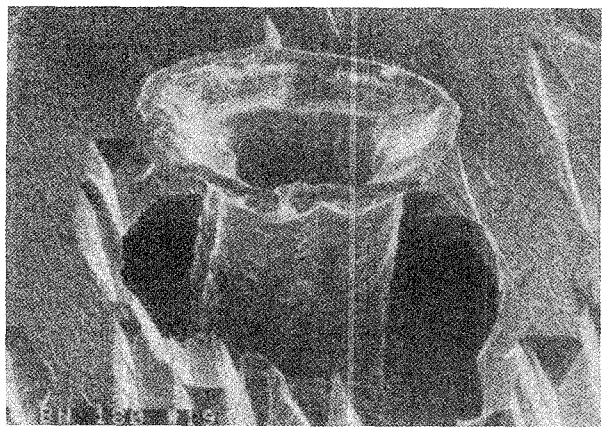

Figure 10. Via Holes Formed Using Laser Drilling; GaAs Material Has Been Etched Away To Show Metal Plating

CONCLUSIONS

The RF-WSI Program is a high risk program with a high potential payoff. Previous work by Westinghouse and McDonnell Douglas has developed much of the technology required to make the present DARPA-funded program successful. Preliminary results from the program are reported in this paper.

ACKNOWLEDGMENTS

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Mr. R. Freitag	- Circuit Lead
Mr. R. Miklosko	- Antenna Lead

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(1) "Manufacturing Technology for Microwave Monolithic Components," Digest of Technical Papers, 1989 U.S. Conference on GaAs Manufacturing Technology.